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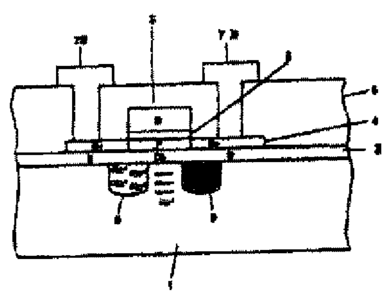
[54]发明名称 薄膜半导体器件

[57]摘要

一种在玻璃基片上形成的能提高薄膜晶体管工作特性和可靠性的薄膜半导体器件。该薄膜半导体器件具有在含有碱性金属的玻璃基片1上形成的薄膜晶体管3。玻璃基片1被缓冲层2覆盖。在这个缓冲层2上形成的薄膜晶体管3具有作为有源层的多晶半导体薄膜4。该缓冲层2包括至少一个氮化硅层，并且能防止薄膜晶体管3被诸如Na的碱性金属沾污，而且具有这样的厚度，它能使薄膜晶体管3免受局部集中的碱性金属离子（Na^+）产生的电场的影响。



权 利 要 求 书

1. 一种薄膜半导体器件，包括：

含有碱性金属的玻璃基片；

覆盖所述玻璃基片表面的缓冲层；以及

在所述缓冲层上形成的薄膜晶体管，并且具有作为有源层的多晶半导体薄膜，

其中所述缓冲区包括至少一个氮化硅层，并防止所述薄膜晶体管被碱性金属沾污，而且具有这样的厚度使得它能够保护所述薄膜晶体管免受局部集中的碱性金属离子产生的电场的影响。

2. 根据权利要求1的薄膜半导体器件，其中所述的氮化硅层具有至少20nm的厚度。

3. 根据权利要求1的薄膜半导体器件，其中所述的缓冲层具有至少100nm的厚度。

4. 根据权利要求1的薄膜半导体器件，其中所述的薄膜晶体管具有背栅结构，包括从底部依次叠加的栅电极，栅绝缘层和多晶半导体薄膜。

5. 根据权利要求4的薄膜半导体器件，其中所述的多晶半导体薄膜在栅电极的正上方具有沟道区，高浓度杂质区位于所述沟道区的每一侧，而低浓度杂质区位于所述沟道区和所述高浓度杂质区之间，所述低浓度杂质区通过所述缓冲层保护免受所述玻璃基片中产生的电场的影响。

6. 根据权利要求4的薄膜半导体器件，其中所述的栅绝缘层包括一个氮化硅层并且与所述缓冲层叠加在一起，两层共同保护和隔离所述薄膜晶体管。

7. 根据权利要求6的薄膜半导体器件，其中相互叠加的栅绝缘层和缓冲层的总厚度至少为100nm。

8. 根据权利要求7的薄膜半导体器件，其中所述的栅绝缘层和缓冲层的总厚度至少为200nm。

9．根据权利要求 1 的薄膜半导体器件，其中所述的缓冲层是由氮化硅层和二氧化硅层构成的双层结构。

10．根据权利要求 1 的薄膜半导体器件，其中形成的象素电极连接到至少所述的薄膜晶体管的一部分。

说　明　书

薄膜半导体器件

本发明涉及一种用作有源阵列液晶显示屏的驱动基片或类似结构的薄膜半导体器件，尤其涉及一种采用普通玻璃作为基片，通过低温工艺制作的薄膜半导体器件。尤其还涉及这样的技术，它用于防止玻璃中含有的碱性金属的有害作用。

薄膜半导体器件是这样的器件，其中薄膜晶体管在绝缘基片上形成，并且由于它们对诸如有源阵列液晶显示屏的驱动基片的应用很理想，所以在最近几年它们有了极大的发展。尤其当在大面积液晶显示屏中使用薄膜半导体器件。对降低绝缘基片的成本是必需的，玻璃基片被用来替代过去使用的相对高质量的石英基片。当使用玻璃基片时，因为它的热阻相当低，所以薄膜晶体管必须在低于600℃的低温工艺中形成。现在用于构成薄膜晶体管的有源层的半导体薄膜，使用的是非晶硅和多晶硅。然而，从薄膜晶体管的工作特性的观点看，多晶硅优于非晶硅。由于这个原因，在最近几年通过低温工艺制作多晶硅薄膜晶体管的发展有了很大的进步。

当多晶硅用作在玻璃基片上形成的薄膜晶体管的有源层时，玻璃基片中含有的碱性金属如钠(Na)引起的沾污就成为一个问题。多晶硅比非晶硅对碱金属沾污更敏感，并且具有这样沾污的多晶硅对薄膜晶体管的工作特性和可靠性具有有害影响。例如，如果碱性金属扩散进入薄膜晶体管的栅绝缘层，器件的特性会改变。当在高温下，施加偏置并且进行工作测试时，器件的特性会发生极大的变化，这是因为栅绝缘层中的碱性金属移动，极化并且在一些位置聚集。因此，当在玻璃基片上制作薄膜晶体管时，在实际制作中预先以氮化硅(SiN_X)膜或含磷玻璃(PSG)作为缓冲层以做基层。通过插入这个缓冲层，从玻璃基片向栅绝缘层的碱性金属的垂直扩散受到抑

制并且防止了栅绝缘层的沾污。

但是已经弄清楚了只是防止碱性金属的垂直运动是不够的。那就是由于施加于薄膜晶体管的驱动电压偏置和碱性金属离子的极化以及其在局部的聚集，在玻璃基片中的碱性金属会产生水平扩散。通过碱性金属离子电荷的局部极化产生一个电场，并且这个电场反过来对薄膜晶体管的工作特性具有有害作用。已经很清楚这样会导致薄膜晶体管的阈值电压和漏电流的波动。要防止玻璃基片中碱性金属的这种水平移动是极其困难的。由于这个原因，例如在USP—5,349,456中公开了一种从玻璃基片中去除Na的方法。然而，这种方法并不总是有实效的，因为它极大削弱了使用低成本玻璃基片的优势。

因此，本发明的目的在于解决上面所述的问题和提供一种在玻璃基片上制作的包括薄膜晶体管的薄膜半导体器件，其中由于玻璃基片中碱性金属的水平扩散导致的上升电场对薄膜晶体管工作特性的有害作用被有效地、便宜地防止。

为了达到上述目的和其它目的，根据本发明的薄膜半导体器件，其基本构成包括含有碱性金属的玻璃基片，覆盖这个玻璃表面的缓冲层和在这个缓冲层上制作的以多晶半导体薄膜为有源层的薄膜晶体管。作为本发明的一个特征部分，缓冲层包括至少一个氮化硅层并且防止薄膜晶体管被碱性金属沾污以及具有保护薄膜晶体管免受由局部碱性金属离子产生的电场的影响的厚度。在本发明的一种形式中，薄膜晶体管具有背栅(bettom gate)结构，其中栅电极，栅绝缘层和半导体薄膜被从底部依次叠放在一起。在这种情况下，半导体薄膜具有位于栅电极正上方的沟道区，高浓度杂质区位于沟道区两端，低浓度杂质区插在沟道区和高浓度杂质区之间。通过缓冲层，低浓度杂质区可免受玻璃基片内形成的电场的影响。更好的是，栅绝缘层包括氮化硅层并且与缓冲层叠加在一起，这两层共同保护和隔离薄膜晶体管。在这种情况下，相互叠放的栅绝缘层和缓冲层的总厚度超过200nm。缓冲层最好是由氮化硅和二氧化硅构成的双层结构。在特定结构中，形成至少连接薄膜晶体管一部分的象素电极，并

且这种薄膜半导体器件能够用于有源阵列显示屏的驱动基片。

本发明中，在玻璃基片和薄膜晶体管之间插入了缓冲层。这个缓冲层包括至少一个氮化硅层，并且能阻碍碱性金属的垂直移动，所以抑制了栅绝缘层的沾污。氮化硅层具有致密的组分，并且通过使它的厚度在 20nm 以上就可以确实完全地防止 Na 和类似碱性金属通过它。加上这个氮化硅层，缓冲层也可以包括例如一个二氧化硅层，具有双层结构。由于二氧化硅层的膜应力低于氮化硅层的膜应力，所以就可能使得缓冲层的整个厚度厚从而使薄膜晶体管与玻璃基片电隔离。通过使缓冲层的厚度至少为 100nm，就可以在电学上保护薄膜晶体管免受玻璃基片的影响。所以就可以保护薄膜晶体管免受由于玻璃基片中碱性金属水平扩散形成的电场的有害作用的影响。结果就是即使使用含有碱性金属的玻璃基片也可以保证薄膜晶体管的可靠性和工作特征。

图 1 是根据本发明的薄膜半导体器件的第一最佳实施方式的截面简图；

图 2 是根据本发明的薄膜半导体器件的第二最佳实施方式的截面简图；

图 3 是根据本发明的薄膜半导体器件的第三最佳实施方式的截面简图；并且

图 4 是根据本发明的薄膜半导体器件组成有源阵列液晶显示屏的例子的透视简图。

参照附图将详细描述本发明的最佳实施方式。图 1 示出了根据本发明的薄膜半导体器件的第一最佳实施方式，并且是一个实例，其中，在玻璃基片上形成了 N 沟、顶栅(top gate)结构的薄膜晶体管。如图 1 所示，这个薄膜半导体器件利用含有诸如钠的碱性金属的玻璃基片 1 制成。玻璃基片 1 的上表面被缓冲层 2 覆盖。在缓冲层 2 上形成薄膜晶体管 3。薄膜晶体管 3 是场效应晶体管，具有作为有源层的含有多晶硅或类似成分的多晶半导体薄膜 4。薄膜晶体管 3 具有顶栅结构，在多晶半导体薄膜 4 上的栅绝缘层 5 之上通过掩膜形成栅电极 G。结果是沟道区 Ch 在栅电极 G 正下方形成，而栅绝

缘层5在它们之间。少量P型杂质扩散进沟道区和多晶半导体薄膜4的一部分，用于调整阈值。源区S和漏区D以高浓度N型杂质注入，形成于沟道区Ch的相对两侧。具有这样的结构的薄膜晶体管3被由PSG或类似成分构成的夹层绝缘层6所覆盖。在夹层绝缘层6内形成接触孔并且通过这些接触孔互连电极7S，7D分别与源区S和漏区D电连接。在这个例子中N型杂质注入形成N沟类型薄膜晶体管3，但是本发明当然不局限于此，也能应用于P沟类型的薄膜晶体管。

作为本发明的特征部分，缓冲层2包括至少一层氮化硅并防止薄膜晶体管3被碱性金属沾污。氮化硅层(SiN_X)具有相对致密的组分，通过使它的厚度至少为20nm就可以确实完全阻碍玻璃基片1中诸如Na这样的碱性金属的向上垂直扩散。该缓冲层2也具有这样的厚度以使它能够保护薄膜晶体管3免受局部碱性金属离子(Na^+)和类似成分导致的电场的影响。例如该缓冲层2具有由氮化硅层(SiN_X)和二氧化硅层(SiO_2)构成的双层结构并且具有至少100nm的总厚度。

作为本发明的一个特征部分，现在对缓冲层2的电场屏蔽功能进行详细描述。当薄膜晶体管3工作时，存在这样的时候例如地电平(0V)施加在源区S一端上的互连电极7S上，并且正向偏置电压施加在连接到漏区D的互连电极7D上。当这种偏置施加到器件时，具有正电荷的Na^+离子从漏区D附近排斥出来并且水平运动到源区S的附近。如附图1所示，其结果是正电荷(Na^+)在源区S附近接近玻璃基片1的表面处聚集，并且形成正电荷区8。同时，在漏区D附近接近玻璃基片1的表面处由于电荷平衡被与排出的Na^+相一致的量打破，形成一个负电荷区9。这样在玻璃基片1的表面的附近，从形成Na^+的位置导致了一个电场。薄膜晶体管3的工作特性受到这个电场的有害影响，结果导致了它的阈值电压的波动和它的漏电流的增加。为了避免这个，本发明中在薄膜晶体管3和玻璃基片1之间插入了缓冲层2。因为缓冲层2具有由SiN_X和SiO_2构成的双层结构并且具有足够的厚度，它确实完全地屏蔽薄膜晶体

管3免受玻璃基片1中形成的电场的影响。此外，因为缓冲层2包括一个SiN_X层，它能以与相关技术相同的方式确实完全阻碍Na的垂直运动，并因此防止了栅绝缘层5的沾污。

图2示出了根据本发明的薄膜半导体器件的第二最佳实施方式并且示出了一个背栅结构的例子。基本结构与如图1所示的第一最佳实施方式的基本结构相同，并且为了便于理解，相对应部分赋予了相同的标号。如图2所示，薄膜晶体管3a具有背栅结构，其中由金属或类似成分制作的栅电极G，栅绝缘层5和多晶半导体薄膜4从底部依次叠加在一起。具有这种结构的薄膜晶体管3a通过缓冲层2与玻璃基片1隔离受到保护。薄膜晶体管3a被夹层绝缘层6覆盖并且在夹层绝缘层6上形成互连电极7S和象素电极10。象素电极10通过接触孔电连接到薄膜晶体管3a的漏区D。具有这种结构的薄膜半导体器件能够用于诸如有源阵列液晶显示屏的驱动基片。即薄膜晶体管3a就作为象素电极10的开关元件来制作。

同如图1所示的具有顶栅的结构一样，具有背栅的结构也是当在漏区D一端施加偏置时，这个偏置的影响会导致玻璃基片1中电荷分布极化的上升并且形成正电荷区和负电荷区。因此，提供了缓冲层2保护薄膜晶体管3a免受玻璃基片1中形成的电场的影响。因为在这种背栅结构情况下，在多晶半导体薄膜4和玻璃基片1之间插入了由金属或类似成分做成的栅电极G，所以半导体薄膜4受玻璃基片1中形成的电场的影响的比例低于顶栅结构的情况。那就是即使在沟道区Ch下面的玻璃基片1中存在Na的偏置，由于除缓冲层2以外还有栅电极G的隔离作用，沟道区Ch本身不太受玻璃基片1中电场的影响。此外，在背栅结构情况下，因为相对于源区S和漏区D之间的偏置，栅电极G上施加的栅电压总是处在源区和漏区之间的电位上，所以玻璃基片1中电荷偏置的存在将不会象顶栅结构上那样大。

图3是根据本发明的薄膜半导体器件的第三最佳实施方式的部分截面图。第三最佳实施方式与如图2所示的第二最佳实施方式基本一致并且为了便于理解，相对应的部分赋予了相同的标号。不同

之处在于第三最佳实施方式中薄膜晶体管具有 LDD(低掺杂漏)结构。如图 3 所示，薄膜晶体管 3a 具有背栅结构，其中栅电极 G，栅绝缘层 5 和多晶半导体薄膜 4 从底部依次叠加在一起。多晶半导体薄膜 4 在栅电极 G 的正上方具有沟道区 Ch，高浓度杂质区(N^+)位于沟道区 Ch 的相对两侧而低浓度杂质区(N)位于沟道区和高浓度杂质区之间。高浓度杂质区(N^+)构成漏区 D，而低浓度杂质区(N)构成 LDD 区。在图 3 中只示出了薄膜晶体管 3a 的漏区 D 端，而源区 S 端省略。在这个例子中，至少 LDD 区被缓冲层 2 屏蔽免受玻璃基片 1 的负电荷区 9 中形成的电场的影响。当在离开栅电极 G 的地方形成 LDD 区时，不同于如图 2 所示的例子，将如图 1 所示的顶栅结构情况，半导体薄膜将受玻璃基片 1 中的电荷的影响。由于这个原因，本例中在玻璃基片 1 和多晶半导体薄膜 4 之间提供了用于削弱电荷影响的缓冲层 2。本例中栅绝缘层 5 包括一个氮化硅层，并与缓冲层 2 叠加，这两层共同保护和隔离薄膜晶体管 3a。相互叠加的栅绝缘层 5 和缓冲层 2 的总厚度超过 200nm。因为在背栅结构中，缓冲层 2 和栅绝缘层 5 叠加，以此获得了共同对电场的隔离作用，所以可以确实完全将 LDD 区与玻璃基片 1 的负电荷区 9 电隔离。

图 4 所示的是一个用如图 2 或图 3 所示的薄膜半导体器件构成的有源阵列液晶显示屏的例子的透视简图。如图 4 所示，液晶显示屏由玻璃制成的驱动基片 101，也由玻璃制成的面基片 102 和夹于两者之间的液晶 103 构成。象素阵列部分 104 和驱动电路部分于驱动基片 101 上形成。驱动电路部分，划分为垂直驱动电路 105 和水平驱动电路 106。还在驱动基片 101 的周边形成了用于外部连接的电极部分 107。电极部分 107 通过互连 108 连接到垂直驱动电路 105 和水平驱动电路 106。象素阵列部分 104 包括相互交叉的栅引线 109 和信号线 110。栅引线 109 连接到垂直驱动电路 105 而信号线 110 连接到水平驱动电路 106。象素电极 111 和用于开关它们的薄膜晶体管 112 形成于线 109 和 110 交叉的地方。虽然没有在附图中示出，但在面基片 102 的内表面上是形成有面电极和颜色滤波器

的。本发明中，普通玻璃材料用作驱动基片101，并且在驱动基片101表面覆盖缓冲层后，在其上形成薄膜晶体管112和象素电极111。并且，同时也形成了垂直驱动电路105和水平驱动电路106。因此由于可以使用便宜的玻璃材料，就可以以相对低的成本制作大面积有源阵列液晶显示屏。此时，因为使用了具有防止碱性金属沾污和电场隔离双重作用的缓冲层，所以没有了玻璃基片对薄膜晶体管可靠性和工作特性有害作用的危险。

如上所述，根据本发明，在玻璃基片和薄膜晶体管之间插入了缓冲层。这个缓冲层包括至少一个氮化硅层，并且在防止薄膜晶体管被碱性金属沾污的同时，它具有这样的厚度能够使薄膜晶体管免受局部集中的碱性金属离子产生的电场的影响。因此就可以避免遭受玻璃基片中的电场的影响并且获得稳定的薄膜晶体管工作特性。并且因为它可以防止薄膜晶体管的碱性金属沾污，所以它的可靠性也提高了。

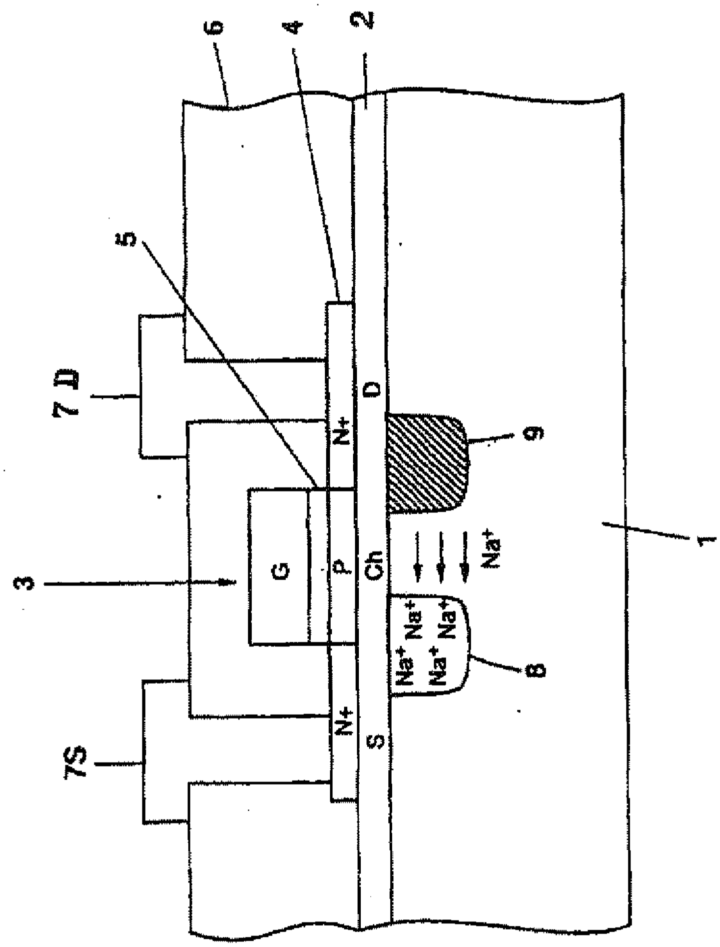


图.1

图.2

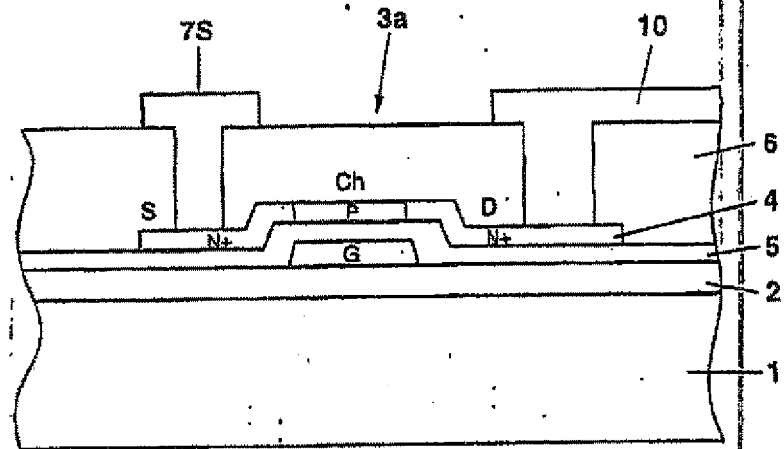


图.3

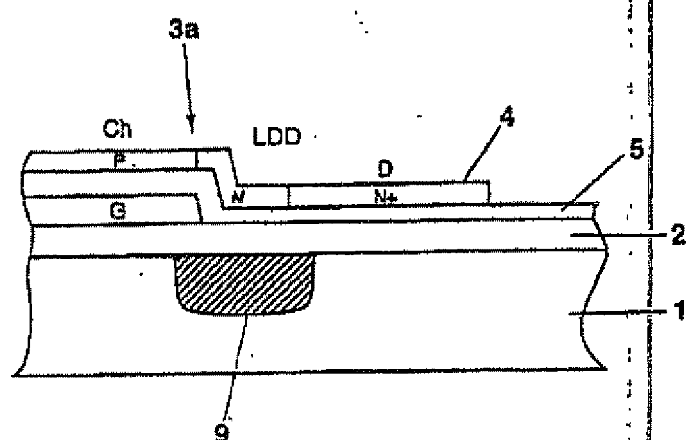
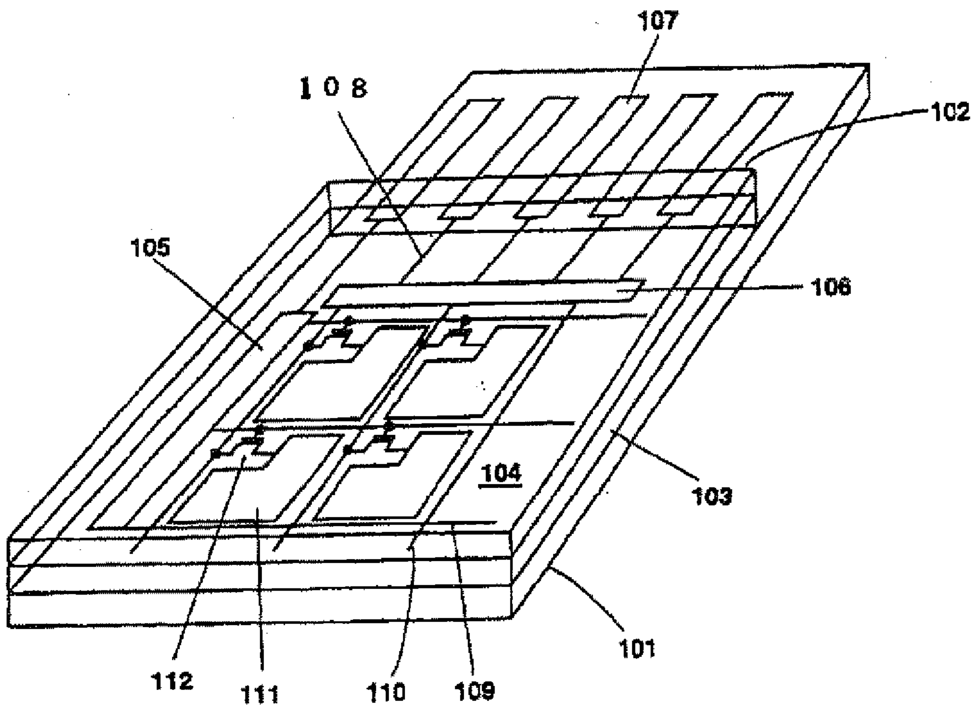


图.4



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(54) **THIN FILM SEMICONDUCTOR DEVICE HAVING A BUFFER LAYER**

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(57) **ABSTRACT**

A thin film semiconductor device having improved operating characteristics and reliability of a thin film transistor formed on a glass substrate. The thin film semiconductor device has a thin film transistor 3 formed on a glass substrate 1 containing alkali metal. The surface of the glass substrate 1 is covered by a buffer layer 2. The thin film transistor 3 formed on this buffer layer 2 has a polycrystalline semiconductor thin film 4 as an active layer. The buffer layer 2 includes at least a silicon nitride film and protects the thin film transistor 3 from contamination by alkali metals such as Na and has a thickness such that it can shield the thin film transistor 3 from an electric field created by localized alkali metal ions (Na^+).

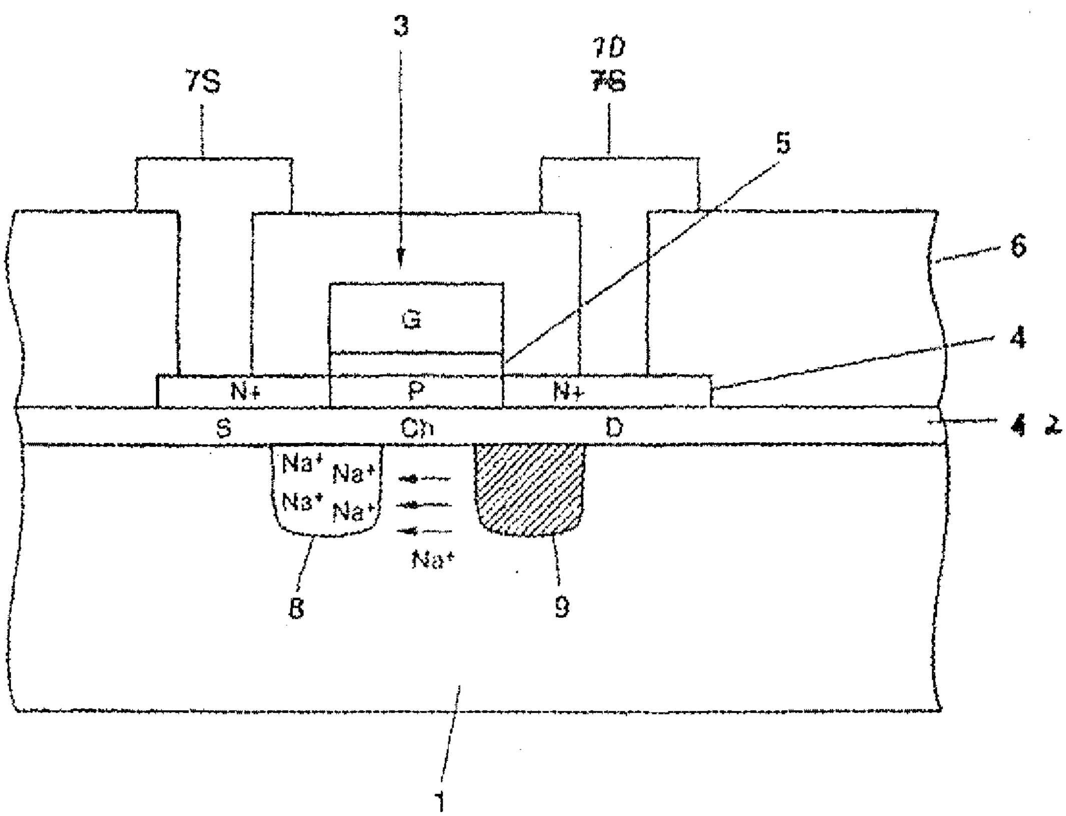


FIG. 1

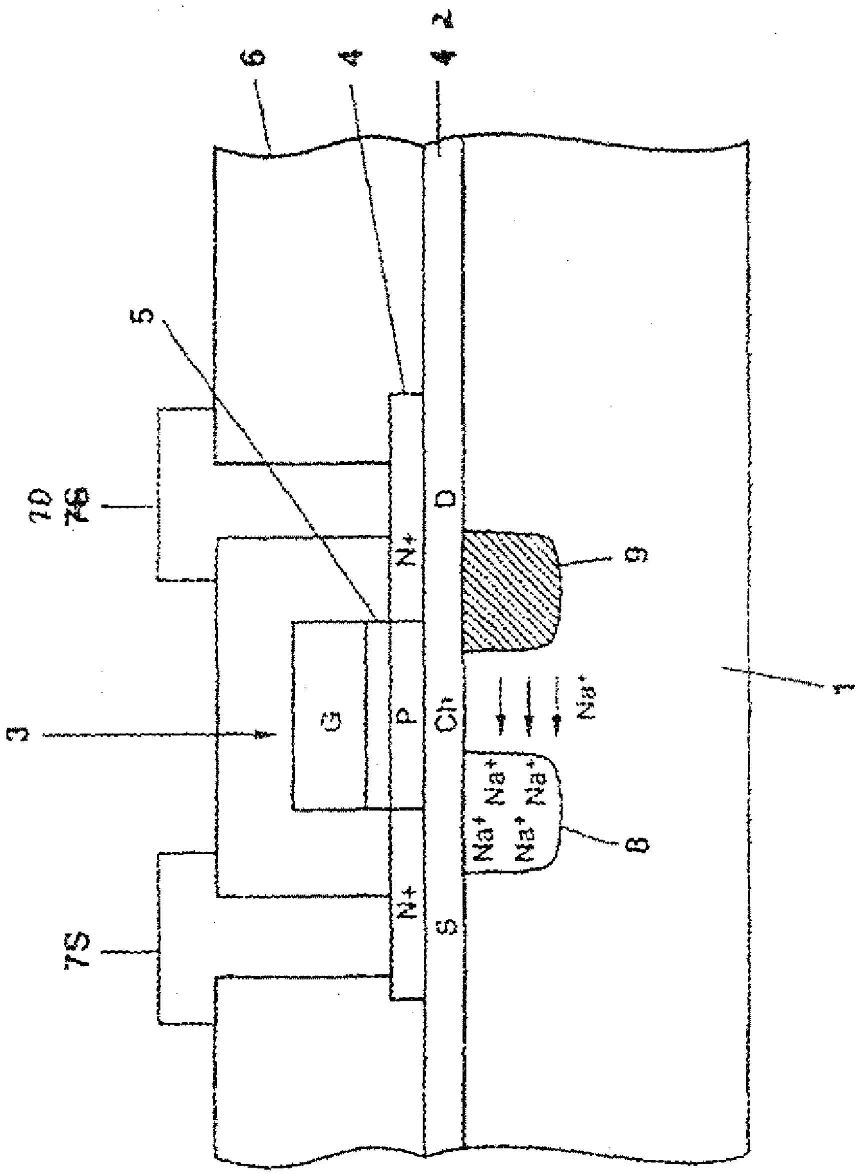


FIG. 2

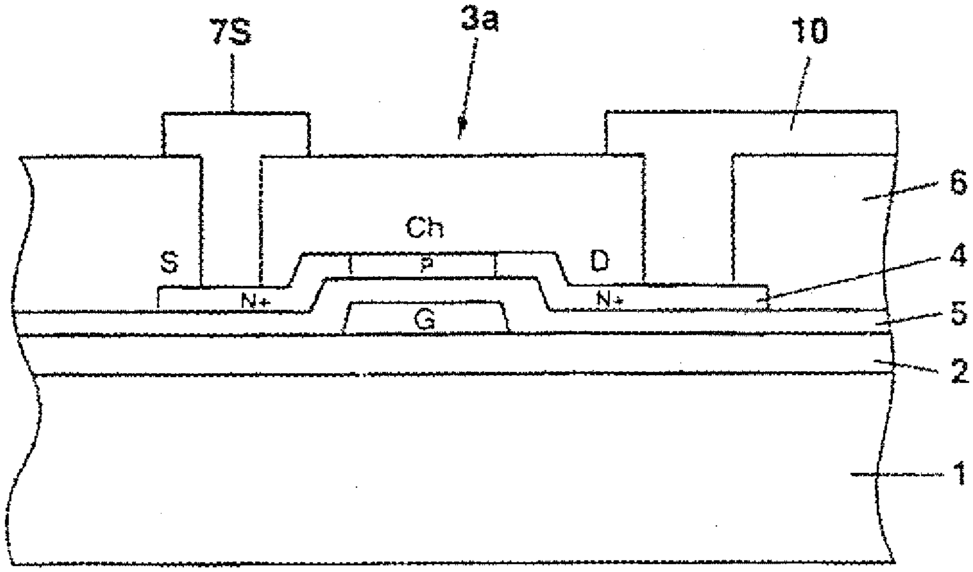


FIG. 3

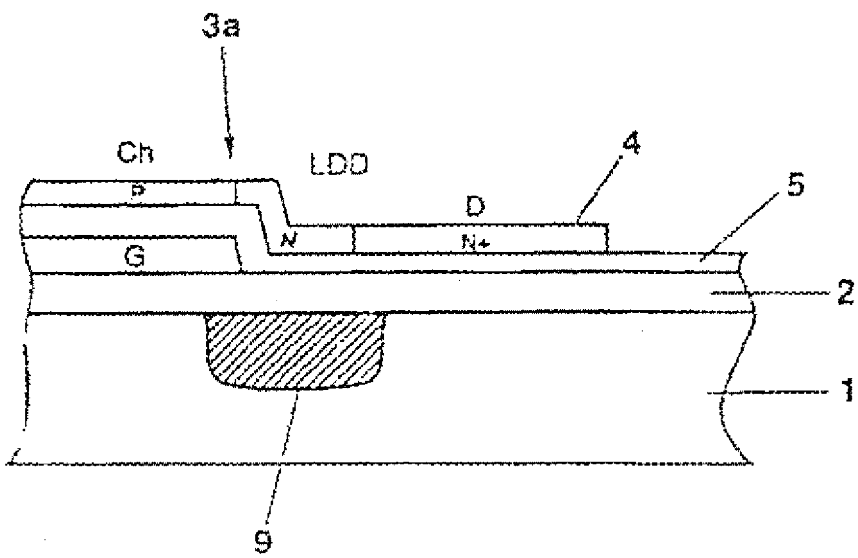
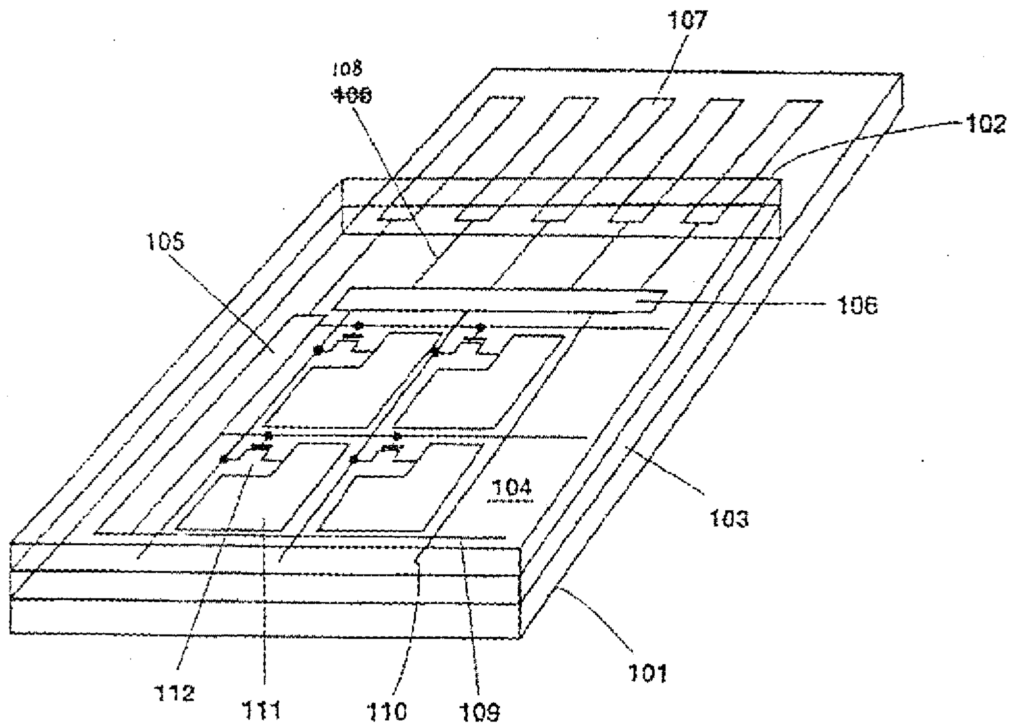


FIG. 4



THIN FILM SEMICONDUCTOR DEVICE HAVING A BUFFER LAYER

BACKGROUND OF THE INVENTION

[0001] This invention relates to a thin film semiconductor device used as a driving substrate of an active matrix liquid crystal display panel or the like. More particularly, it relates to a thin film semiconductor device using ordinary glass as a substrate and made by low temperature processes. Still more particularly, it relates to technology for preventing adverse affects of alkali metals contained in the glass.

[0002] A thin film semiconductor device is a device wherein a thin film transistor is formed on an insulating substrate, and because they are ideal for example for driving substrates of active matrix liquid crystal display panels their development has been being advanced vigorously in recent years. Particularly when using a thin film semiconductor device in a large-area liquid crystal display panel, it is essential to reduce the cost of the insulating substrate, and glass substrates are being employed instead of the relatively high quality quartz substrates used in the past. When a glass substrate is used, because its heat resistance is relatively low, the thin film transistors must be formed by low temperature processes of below 600° C. Now, as a semiconductor thin film constituting active layers of the thin film transistors, amorphous silicon and polycrystalline silicon have been used. However, from the point of view of the operating characteristics of the thin film transistors, polycrystalline silicon is superior to amorphous silicon. For this reason, the development of polycrystalline silicon thin film transistors made by low temperature processes has been being advanced in recent years.

[0003] When polycrystalline silicon is used as an active layer of a thin film transistor formed on a glass substrate, contamination caused by alkali metals such as sodium (Na) contained in the glass substrate has been a problem. Polycrystalline silicon is more sensitive to alkali metal contamination than amorphous silicon, and with polycrystalline silicon such contamination has an adverse influence on the operating characteristics and reliability of the thin film transistor. For example, if an alkali metal diffuses into the gate insulating film of a thin film transistor the device characteristics change. When at a high temperature a bias is applied and an operating test is carried out, the device characteristics change greatly because alkali metal in the gate insulating film moves and polarizes and concentrates in localities. Consequently, when thin film transistors have been formed on a glass substrate, the practice of forming in advance as a base layer a silicon nitride film (SiN_x) or a phosphorus-containing glass (PSG) as a buffer layer has been carried out. By this buffer layer being interposed, the vertical diffusion of alkali metal from the glass substrate toward the gate insulating film is suppressed and contamination of the gate insulating film is prevented.

[0004] However, it has become clear that just preventing vertical movement of alkali metal is not sufficient. That is, horizontal diffusion of alkali metal included in the glass substrate occurs due to bias of the driving voltage impressed on the thin film transistor, and alkali metal ions polarize and concentrate locally. An electric field is created by local polarization of charges of alkali metal ions, and this reversely has an adverse affect on the operating characteristics of the thin film transistor. It has become clear that as a result of this the threshold voltage and the leak current of the thin film transistor undergo fluctuations. It is extremely difficult to prevent this horizontal movement of alkali metal in the glass substrate. For this reason, for example in U.S. Pat. No. 5,349,456 a method for removing Na from a glass substrate is disclosed. However, this method is not always practical because it greatly diminishes the merit of using a low cost glass substrate.

SUMMARY OF THE INVENTION

[0005] Accordingly, it is an object of the invention to solve the problem described above and provide a thin film semiconductor device comprising a thin film transistor formed on a glass substrate wherein an electric field arising as a result of horizontal diffusion of alkali metal in the glass substrate is effectively and cheaply prevented from adversely affecting the operating characteristics of the thin film transistor.

[0006] To achieve the above-mentioned object and other objects, a thin film semiconductor device according to the invention comprises as a basic construction a glass substrate containing an alkali metal, a buffer layer covering the surface of the glass substrate and a thin film transistor formed on the buffer layer with a polycrystalline semiconductor thin film as an active layer. As a characterizing feature of the invention, the buffer layer includes at least a silicon nitride film and protects the thin film transistor from alkali metal contamination and has a thickness such that it ca n shield the thin film transistor from an electric field created by localized alkali metal ions. In one form of the invention, the thin film transistor has a bottom gate structure wherein a gate electrode, a gate insulating film and a semiconductor thin film are superposed in order from the bottom. In this case, the semiconductor thin film has a channel region located directly above the gate electrode, high concentration impurity regions located on either side of the channel region and low concentration impurity regions interposed between the channel region and the high concentration impurity regions. The low concentration impurity regions are shielded from an electric field forming in the glass substrate by the buffer layer. Preferably, the gate insulating film includes a silicon nitride layer and is superposed with the buffer layer and the two synergetically protect and shield the thin film transistor. In this case, the total thickness of the mutually superposed gate insulating film and buffer layer is over 200 nm. The buffer layer is preferably a two-layer structure made up of a silicon nitride film and a silicon oxide film. In a specific construction, a pixel electrode is formed connected to at least a part of the thin film transistor and the thin film semiconductor device can be used in a driving substrate of an active matrix display panel.

[0007] In the invention, a buffer layer is interposed between a glass substrate and a thin film transistor. This buffer layer includes at least a silicon nitride film, and blocks vertical movement of alkali metal and thereby suppresses contamination of the gate insulating film. The silicon nitride film has a fine composition, and by making its thickness above 20 nm it is possible to substantially completely prevent Na and the like from passing through it. Also, in addition to the silicon nitride film this buffer layer includes for example a silicon oxide film and has a two-layer structure. Because film stresses in the silicon oxide film are smaller than in the silicon nitride film it is possible to make

the thickness of the buffer layer as a whole large and thereby electrically separate the thin film transistor from the glass substrate. By making the thickness of the buffer layer at least 100 nm it is possible to electrically shield the thin film transistor from the glass substrate. Therefore, it is possible to shield the thin film transistor from adverse affects of an electric field formed as a result of horizontal diffusion of alkali metal inside the glass substrate. As a result, it becomes possible to maintain the reliability and operating characteristics of the thin film transistor even when a glass substrate containing alkali metal is used.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] **FIG. 1** is a schematic sectional view of a first preferred embodiment of a thin film semiconductor device according to the invention;

[0009] **FIG. 2** is a schematic sectional view of a second preferred embodiment of a thin film semiconductor device according to the invention;

[0010] **FIG. 3** is a schematic sectional view of a third preferred embodiment of a thin film semiconductor device according to the invention; and

[0011] **FIG. 4** is a schematic perspective view of an example of an active matrix liquid crystal display panel assembled using a thin film semiconductor device according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0012] Preferred embodiments of the invention will now be described in detail with reference to the accompanying drawings. **FIG. 1** shows a first preferred embodiment of a thin film semiconductor device according to the invention, and is an example wherein a thin film transistor of N-channel type and of top gate structure is formed on a glass substrate. As shown in **FIG. 1**, this thin film semiconductor device is made using a glass substrate 1 containing an alkali metal such as Na. The upper surface of the glass substrate 1 is covered by a buffer layer 2. A thin film transistor 3 is formed on the buffer layer 2. The thin film transistor 3 is a field effect transistor having a polycrystalline semiconductor thin film **4** consisting of polycrystalline silicon or the like as an active layer. The thin film transistor **3** has a top gate structure, and a gate electrode G is formed by patterning on a gate insulating film **5** on the polycrystalline semiconductor thin film **4**. As a result, a channel region Ch is formed directly below the gate electrode G with the gate insulating film **5** therebetween. A small amount of a P-type impurity is diffused into this channel region Ch part of the polycrystalline semiconductor thin film **4** for threshold value adjustment. A source region S and a drain region D impregnated with an N-type impurity at a high concentration are provided on opposite sides of the channel region Ch. The thin film transistor 3 having this construction is covered with an interlayer insulating film **6** consisting of PSG or the like. Contact holes are formed in the interlayer insulating film **6**, and through these contact holes interconnection electrodes 7S, 7D are electrically connected to the source region S and the drain region D respectively. In this example an N-type impurity is injected to form an N-channel type thin film transistor **3**, but of course the invention is not limited to this and can also be applied to a P-channel type thin film transistor.

[0013] As a characterizing feature of the invention the buffer layer **2** includes at least a silicon nitride film, and protects the thin film transistor **3** from alkali metal contamination. The silicon nitride film (SiN_x) has a relatively fine composition, and by making its thickness at least 20 nm it is possible to substantially completely block the vertical upward diffusion of alkali metals such as Na contained in the glass substrate **1**. Also, this buffer layer **2** has a thickness such that it can shield the thin film transistor **3** from an electric field resulting from localized alkali metal ions (Na^+) and the like. For example the buffer layer **2** has a two-layer structure made up of the silicon nitride film (SiN_x) and a silicon oxide film (SiO_2) and has a total thickness of at least 100 nm.

[0014] The electric field shielding function of the buffer layer **2**, which is a characterizing feature of the invention, will now be described in more detail. When the thin film transistor **3** is operated, there are times when for example a ground potential (0V) is impressed on the interconnection electrode **7S** on the source region S side and a positive bias voltage is impressed on the interconnection electrode **7D** connected to the drain region D. When this kind of bias is applied to the device, Na^+ ions, which are positive charges, are excluded from the vicinity of the drain region D and move horizontally to the vicinity of the source region S. As a result, as shown in **FIG. 1**, positive charges (Na^+) concentrate in the vicinity of the source region S near the surface of the glass substrate **1** and a positive region **8** is formed. Meanwhile, in the vicinity of the drain region D near the surface of the glass substrate **1**, because the charge equilibrium breaks down by an amount corresponding to the exclusion of the Na^+, a negative region **9** is formed. In this way an electric field resulting from localization of Na^+ forms in the vicinity of the surface of the glass substrate **1**. The operating characteristics of the thin film transistor **3** are adversely affected by this electric field, resulting in fluctuation of its threshold voltage and increase of its leakage current. To avoid this, in this invention the buffer layer **2** is interposed between the thin film transistor **3** and the glass substrate **1**. Because this buffer layer **2** has a two-layer structure made up of SiN_x and SiO_2 and has an ample thickness, it substantially completely shields the thin film transistor **3** from electric fields forming in the glass substrate **1**. Furthermore, because the buffer layer **2** includes an SiN_x film, it substantially completely blocks vertical movement of Na in the same way as in the related art and thereby prevents contamination of the gate insulating film **5**.

[0015] **FIG. 2** shows a second preferred embodiment of a thin film semiconductor device according to the invention, and shows an example of a bottom gate structure. The basic structure is the same as that of the first preferred embodiment shown in **FIG. 1**, and corresponding parts have been given the same reference numerals to facilitate understanding. As shown in **FIG. 2**, a thin film transistor **3a** has a bottom gate structure wherein a gate electrode G made of metal or the like, a gate insulating film **5** and a polycrystalline semiconductor thin film **4** are superposed in order from the bottom. The thin film transistor **3a** having this construction is protected and shielded from the glass substrate **1** by a buffer layer **2**. The thin film transistor **3a** is covered by an interlayer insulating film **6**, and an interconnection electrode **7S** and a pixel electrode **10** are formed on the interlayer insulating film **6**. The pixel electrode **10** is electrically connected to the drain region D of the thin film

transistor 3*a* through a contact hole. A thin film semiconductor device having this construction can be used for example in a driving substrate of an active matrix liquid crystal display panel. That is, the thin film transistor 3*a* is formed as a switching element of a pixel electrode **10**.

[0016] With the bottom gate structure also, as with the top gate structure shown in **FIG. 1**, when a bias is impressed on the drain region D side the influence of this bias causes a polarization of the charge distribution in the glass substrate **1** to arise and a positive region and a negative region form. Therefore, the buffer layer **2** is provided to shield the thin film transistor 3*a* from the influence of electric fields forming in the glass substrate **1**. Because in the case of the bottom gate structure the gate electrode G made of metal or the like is interposed between the polycrystalline semiconductor thin film **4** and the glass substrate **1**, the proportion of the semiconductor thin film **4** affected by electric fields forming inside the glass substrate **1** is less than in the case of the top gate structure. That is, even if a biased presence of Na were to occur inside the glass substrate **1** below the channel region Ch, because in addition to the buffer layer **2** there is a shielding effect of the gate electrode G, the channel region Ch itself is not so affected by the electric field in the glass substrate **1**. Furthermore, in the case of the bottom gate structure, because with respect to the bias between the source region S and the drain region D the gate voltage impressed on the gate electrode G is always at a potential level between the source region and the drain region, biased presences of charges inside the glass substrate **1** would not be expected to occur as much as in the case of the top gate structure.

[0017] **FIG. 3** is a partial sectional view of a third preferred embodiment of a thin film semiconductor device according to the invention. This third preferred embodiment is basically the same as the second preferred embodiment shown in **FIG. 2**, and corresponding parts have been given the same reference numerals to facilitate understanding. The point of difference is that in this third preferred embodiment the thin film transistor has an LDD (Lightly Doped Drain) structure. As shown in **FIG. 3**, the thin film transistor 3*a* has a bottom gate structure wherein a gate electrode G, a gate insulating film **5** and a polycrystalline semiconductor thin film **4** are superposed in order from the bottom. The polycrystalline semiconductor thin film **4** has a channel region Ch located directly above the gate electrode G, high concentration impurity regions (N+) located on opposite sides of the channel region Ch and low concentration impurity regions (N) located between the channel region and the high concentration impurity regions. A high concentration impurity region (N+) constitutes a drain region D, and a low concentration impurity region (N) constitutes an LDD region. In **FIG. 3** only the drain region D side of the thin film transistor 3*a* is shown, and the source region S side is omitted. In this example at least the LDD region is shielded from an electric field forming in the negative region **9** of the glass substrate **1** by a buffer layer **2**. When an LDD region is formed away from the gate electrode G, unlike the example shown in **FIG. 2**, as in the case of the top gate structure shown in **FIG. 1** the semiconductor thin film is influenced by charges inside the glass substrate **1**. For this reason, in this example the buffer layer **2** for weakening the influence of charges is provided between the glass substrate **1** and the polycrystalline semiconductor thin film **4**. In this example the gate insulating film **5** includes a silicon nitride layer and is superposed with the buffer layer **2** and the two synergetically protect and shield the thin film transistor 3*a*. The total thickness of the mutually superposed gate insulating film **5** and buffer layer **2** is over 200 nm. Because in the bottom gate structure the buffer layer **2** and the gate insulating film **5** are superposed and a synergetic electric field shielding effect is obtained in this way, it is possible to electrically separate the LDD region from the negative region **9** of the glass substrate **1** substantially completely.

[0018] **FIG. 4** is a schematic perspective view showing an example of an active matrix liquid crystal display panel assembled using the thin film semiconductor device shown in **FIG. 2** or **FIG. 3**. As shown in **FIG. 4**, the liquid crystal display panel is made up of a driving substrate **101** made of glass, a facing substrate **102** also made of glass and a liquid crystal **103** held between the two. A pixel array part **104** and a driving circuit part are formed on the driving substrate **101**. The driving circuit part is divided into a vertical driving circuit **105** and a horizontal driving circuit **106**. Also, terminal parts **107** for outside connections are formed on a peripheral part of the driving substrate **101**. The terminal parts **107** are connected to the vertical driving circuit **105** and the horizontal driving circuit **106** by way of interconnections **108**. The pixel array part **104** comprises mutually intersecting gate lines **109** and signal lines **110**. The gate lines **109** are connected to the vertical driving circuit **105** and the signal lines **110** are connected to the horizontal driving circuit **106**. Pixel electrodes **111** and thin film transistors **112** for switching these are formed at the intersections of the lines **109**, **110**. Although not shown in the drawing, facing electrodes and color filters are formed on the inner surface of the facing substrate **102**. In this invention an ordinary glass material is used as the driving substrate **101**, and the thin film transistors **112** and the pixel electrodes **111** are formed on the driving substrate **101** after the surface thereof is covered with a buffer layer. Also, the vertical driving circuit **105** and the horizontal driving circuit **106** are formed at the same time. Therefore, because it is possible to use a cheap glass material, it is possible to make a large-area active matrix liquid crystal display panel at a relatively low cost. At this time, because a buffer layer having both an alkali metal contamination preventing function and an electric field shielding function is used, there is no risk of the glass substrate adversely affecting the reliability or operating characteristics of the thin film transistors.

[0019] As described above, according to the invention, a buffer layer is interposed between a glass substrate and a thin film transistor. This buffer layer includes at least a silicon nitride film, and as well as protecting the thin film transistor from alkali metal contamination it has a thickness such that it can shield the thin film transistor from an electric field created by localized alkali metal ions. Consequently, it is possible to avoid suffering the effects of electric fields inside the glass substrate and obtain stable thin film transistor operating characteristics. Also, because it is possible to prevent alkali metal contamination of the thin film transistor, its reliability is improved.

What is claimed is:

1. A thin film semiconductor device comprising:

a glass substrate containing an alkali metal;

a buffer layer covering the surface of said glass substrate; and

a thin film transistor formed on said buffer layer and having a polycrystalline semiconductor thin film as an active layer,

wherein said buffer layer includes at least a silicon nitride film and protects said thin film transistor from alkali metal contamination and has a thickness such that it can shield said thin film transistor from an electric field created by localized alkali metal ions.

2. A thin film semiconductor device according to claim 1, wherein said silicon nitride film has a thickness of at least 20 nm.

3. A thin film semiconductor device according to claim 1, wherein said buffer layer has a thickness of at least 100 nm.

4. A thin film semiconductor device according to claim 1, wherein said thin film transistor has a bottom gate structure comprising a gate electrode, a gate insulating film and a polycrystalline semiconductor thin film superposed in order from the bottom.

5. A thin film semiconductor device according to claim 4, wherein said polycrystalline semiconductor thin film has channel region located directly above the gate electrode, high concentration impurity regions located on either side of said channel region and low concentration impurity regions located between said channel region and said high concentration impurity regions, said low concentration impurity regions being shielded from an electric field arising in said glass substrate by said buffer layer.

6. A thin film semiconductor device according to claim 4, wherein said gate insulating film contains a silicon nitride layer and is superposed with said buffer layer and the two synergetically protect and shield said thin film transistor.

7. A thin film semiconductor device according to claim 6, wherein the total thickness of the mutually superposed gate insulating film and buffer layer is at least 100 nm.

8. A thin film semiconductor device according to claim 7, wherein the total thickness of said gate insulating film and buffer layer is at least 200 nm.

9. A thin film semiconductor device according to claim 1, wherein said buffer layer is of a two-layer structure made up of a silicon nitride film and a silicon oxide film.

10. A thin film semiconductor device according to claim 1, wherein a pixel electrode is formed connected to at least a part of said thin film transistor.

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